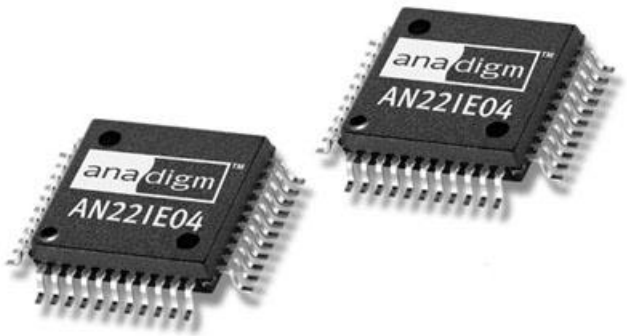
AN221E04 Datasheet

Enhanced I/O Dynamically Reconfigurable FPAA



PRELIMINARY INFORMATION

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This information is preliminary information — subject to change

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PRODUCT AND ARCHITECTURE OVERVIEW

The AN221E04 device consists of a 2x2 matrix of fully Configurable Analog Blocks (CABs), surrounded by a fabric of programmable interconnect resources. Configuration data is stored in an on-chip SRAM configuration memory. Compared with the first-generation FPAAs, the Anadigmvortex architecture provides a significantly improved signal-to-noise ratio as well as higher bandwidth. These devices also accommodate nonlinear functions such as sensor response linearization and arbitrary waveform synthesis.

The AN221E04 device features an advanced input/output structure that allows the FPAA to be programmed with up to six outputs – or triple the number provided by the ANx20E04 devices. The AN221E04 devices have four configurable I/O cells and two dedicated output cells. For I/O-intensive applications, this means a single FPAA can now be used to process multiple channels of analog signals where two or more such devices were previously needed.

In addition, the AN221E04 devices allow designers to implement an integrated 8-bit analog-to-digital converter on the FPAA, eliminating the potential need for an external converter. Using this new device, designers can route the digital output of the A/D converter off-chip using one of the dedicated output cells.

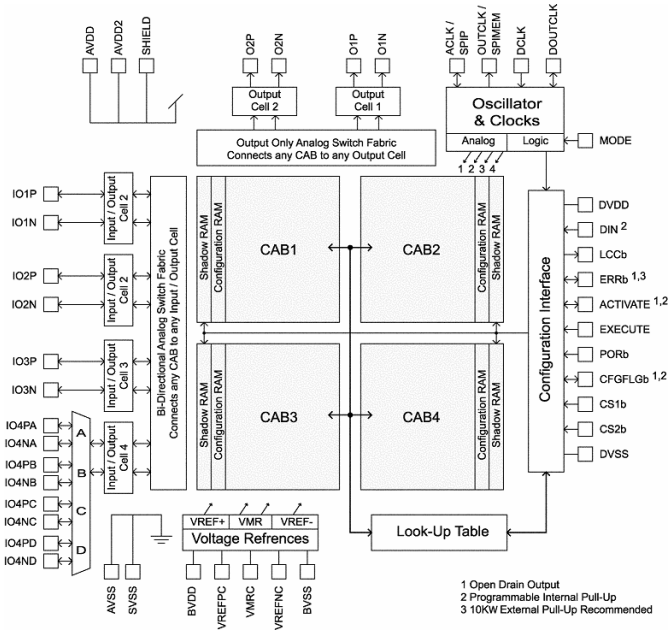


Figure 1: Architectural overview of the AN221E04 device

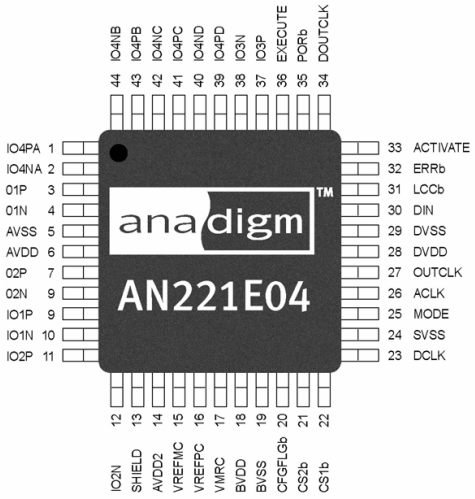
With dynamic reconfigurability, the functionality of the AN221E04 can be reconfigured in-system by the designer or on-the-fly by a microprocessor. A single AN221E04 can thus be programmed to implement multiple analog functions and/or to adapt on-the-fly to maintain precision operation despite system degradation and aging.

PRODUCT FEATURES

- **Dynamic reconfiguration**
- **Four configurable I/O cells, two dedicated output cells**
- **8-bit SAR analog-to-digital converter**
- Fully differential architecture
- Fully differential I/O buffering with options for single ended to differential conversion
- Low input offset through chopper stabilized amplifiers
- 256 Byte Look-Up Table (LUT) for linearization and arbitrary signal generation
- 4:1 Input multiplexer
- Typical Signal Bandwidth: DC-2MHz (Bandwidth is CAM dependent)
- Signal to Noise Ratio (SNR, target only):
  - o Broadband 80dB
  - o Narrowband (audio) 100dB
- Total Harmonic Distortion (THD): 80dB
- DC offset <100µV
- Package: 44-pin QFP (10x10x2mm)
  - o Lead pitch 0.8mm
- Supply voltage: 5V

APPLICATIONS

- Real-time software control of analog system peripherals
- Intelligent Sensors
- Adaptive filtering and control
- Adaptive DSP front-end
- Adaptive industrial control and automation
- Self-calibrating systems
- Compensation for ageing of system components
- Dynamic recalibration of remote systems
- Ultra-low frequency signal conditioning
- Custom analog signal processing



ORDERING CODES

AN221E04-QFPSP	Dynamically reconfigurable FPAA Sample Pack
AN221E04-QFPTY	Dynamically reconfigurable FPAA Tray (96 pcs)
AN221E04-QFPTR	Dynamically reconfigurable FPAA Tape & Reel (1000 pcs)
AN221D04-EVAL	AN221E04 Evaluation Kit
AN221D04-DEVLP	AN221E04 Development Kit

[*For more detailed information on the features of the AN221E04 device, please refer to the AN121E04/AN221E04 User Manual*]

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC power supplies	AVDD(2) BVDD DVDD	-0.5	-	5.5 V	V	AVSS, BVSS, DVSS and SVSS all held to 0.0 V [a]
xVDD to xVDD offset		-0.5		0.5	V	Ideally all supplies should be at the same voltage
Package power dissipation	Pmax 25°C Pmax 85°C	-	-	1.8 0.73	W	Still air, no heatsink, 4 layer board, 44 pins. θja = 55°C/W
Analog and digital input voltage	Vinmax	VSS-0.5	-	VDD+0.5	V	
Ambient operating temperature	Top	-40	-	85	°C	
Storage temperature	Tstg	-65		150	°C	

[a] Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for Vdd of up to 7 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC power supplies	AVDD(2) BVDD DVDD	4.75	5.00	5.25	V	AVSS, BVSS, DVSS and SVSS all held to 0 V
Analog input voltage	Vina	VMR-1.9	-	VMR+1.9	V	VMR is 2.0 volts above AVSS
Digital input voltage	Vind	0	-	DVDD	V	
Junction temp	Tj	-40	-	125	°C	Assume a package θja = 55°C/W [b]

[b] Nearly every aspect of the internal circuitry of the device is programmable, in order to calculate the junction temperature you must first empirically determine the current draw (total Idd) for the design. Once the current consumption established then the following formula can be used; Tj = Ta + Idd x Vdd x 55 °C/W, where Ta is the ambient temperature. The worst case θja of 55°C/W assumes no air flow and no additional heatsink of any type.

Digital I/O Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input voltage low	Vih	0	-	30	-	% of DVDD
Input voltage high	Vil	70	-	100	-	% of DVDD
Output voltage low	Vol	0	-	20	-	% of DVDD
Output voltage high	Voh	80	-	100	-	% of DVDD
Input leakage current	Iil	-	-	±1.0	µA	All pins except DCLK
Input leakage current	Iil	-	±12.0	-	µA	DCLK if a crystal is connected and the on-chip oscillator is used
Max. capacitive load	Cmax	-	-	10	pF	The maximum load for a digital output is 10 pF || 10 Kohm
Min. resistive load	Rmin	10	-	-	Kohm	The maximum load for a digital output is 10 pF || 10 Kohm
DCLK frequency	Fmax	-	-	40	MHz	For MODE = 1, Max DCLK is 16 MHz
ACLK frequency	Fmax	-	-	40	MHz	Divide down to < 16 MHz prior to use as a CAB clock
Clock duty cycle	-	45	-	55	%	All clocks

Analog Inputs General

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High precision input range [c]	Vina	0.5	-	3.5	V	VMR +/- 1.5v
Reduced precision input range [d]	Vina	0.1	-	3.9	V	VMR +/- 1.9v
High precision differential input [c]	Vdiffina	0	-	+/-3.0	V	Common mode voltage = 2 V
Reduced precision differential input [d]	Vdiffina	0	-	+/-3.8	V	Common mode voltage = 2 V
Common mode input range	Vcm	1.8	2.0	2.2	V	
Input offset	Vos	-	5	15	mV	Non-chopper stabilized input
Input frequency	Fain	0	<2	8	MHz	Max value is clock, CAM and input stage dependant
Noise figure	Noise	-	TBD	-	nV/sqrtHz	See typical graphical data provided later in this document
Signal-to noise ratio and distortion	SINAD	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660Hz • See typical graphical data provided later in this document
Spurious free dynamic range	SFDR	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660Hz • See typical graphical data provided later in this document

c High precision operating range provides optimal linearity and dynamic range
d Reduced precision operating range provides maximum dynamic range and reduced linearity

Input Differential Amplifier ON and Filter OFF

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above				Usable input range will be reduced by the effective gain setting
Gain setting	Ginamp	16	-	128		
Gain accuracy		-	1.0	2.5	%	
Gain accuracy drift	Dist	-	-	0.5	%	This value is theoretical and not measured
Equivalent input offset voltage	Vos	-	3	12	mV	• Non-chopper stabilized input • When the input amplifier and filter are used in combination Vos contribution comes only from the input amplifier
Offset voltage temperature coefficient	Voffsettc	-	1	10	µV/°C	from -40°C to 125°C
High precision input frequency [c]	Fain	0	-	2	MHz	
Reduced precision input frequency [d]	Fain	0	<2	8	MHz	
Power supply rejection ratio	PSRR	65	-	-	dB	d.c. Amp Gain =16 a.c. See graphs
Large signal harmonic distortion	Dist	-	65	-	dB	0.4v p-p Differential input at 660Hz Gain setting = 16
Input resistance	Rin	10		-	Mohm	
Input capacitance	Cin	-		5.0	pF	

c High precision operating range provides optimal linearity and dynamic range
d Reduced precision operating range provides maximum dynamic range and reduced linearity

Input Differential Chopper Amplifier ON and Filter OFF

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above				Usable input range will be reduced by the effective gain setting
Gain setting	Ginamp	16	-	128		
Gain accuracy		-	1.0	2.5	%	
Gain accuracy drift		-	-	0.5	%	This value is theoretical and not measured
Chopper clock range	Chclk	Fc/260100	<250	>250	kHz	• Fc = master clock frequency • Always use as slow as possible • Fc > 250kHz will result in some signal attenuation
Equivalent input offset voltage	Vos	-	<100	200	µV	• Chopper stabilized amplifier • The maximum value of 200µV is guaranteed by production test • This is a tester limitation
Offset voltage temperature coefficient	Voffsettc	-	0.5	2.0	µV/°C	from -40°C to 125°C
Power supply rejection ratio	PSRR	65	-	-	dB	d.c. a.c. See graphs
Large signal harmonic distortion	Dist	-	40	-	dB	0.4v p-p Differential input at 660Hz Gain setting = 16
Input frequency	Fain	0	Fch/20	Fch/2	MHz	• Fch=Chopper clock frequency • The chopper frequency and input frequency should be chosen such that subsequent low pass filtering can remove the chopper stage frequency elements
Input resistance	Rin	10		-	Mohm	Input to filter or chopper
Input capacitance	Cin	-		5.0	pF	

Input Differential Amplifier OFF and Filter ON

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above				
Equivalent input offset	Vos	-	8	32	mV	Non-chopper stabilized input, Filter corner frequency =470kHz
Offset voltage temperature coefficient	Voffsettc	-	0.05 [I]	1.0 [II]	mV/°C	from -40°C to 125°C I. measured at filter corner = 470kHz II. maximum at Filter corner =76kHz
Input frequency	Fain	-	-	-	MHz	• Input filter frequency will define the maximum frequency • Input filter is recommended to be >30x higher than the max input frequency, for 80dB distortion performance
Power supply rejection ratio	PSRR	68	-	-	dB	d.c. a.c. See graphs
Large signal harmonic distortion	Dist	-	82	-	dB	4v p-p differential input at 660Hz Filter corner frequency 470kHz
Input low pass filter (anti-alais) corner frequency settings	Ffiltcorner	76	-	470	kHz	
Input resistance	Rin	10	-	-	Mohm	Input to filter or chopper
Input capacitance	Cin	-	-	5.0	pF	

Input Differential Voltage Mode, Amplifier OFF, Filter OFF and Unity Gain Stage ON

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above			V	
Equivalent input offset	Vos	-	5	15	mV	Non-chopper stabilized input
Offset voltage temperature coefficient	Voffsettc	-	20	50	µV/°C	from -40°C to 125°C
Input frequency	Fain	-	-	1.0	MHz	Gain bandwidth limited by input impedance
Power supply rejection ratio	PSRR	60	-	-	dB	d.c. a.c. graphs
Large signal harmonic distortion	Dist	-	80	-	dB	4v p-p differential input at 660Hz
Large signal harmonic distortion	Dist	-	80	-	dB	3v p-p single ended signal at 660Hz
Input resistance	Rin	-	126	-	Kohm	Input to unity gain stage
Input capacitance	Cin	-	2.0	5.0	pF	

Input Differential Voltage Mode, Amplifier OFF, Filter OFF and Unity Gain Stage OFF

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above			V	
Equivalent input offset	Vos	N/A	N/A	N/A	mV	See CAM Op Amp
Offset voltage temperature coefficient	Voffsettc	N/A	N/A	N/A	µV/°C	See CAM Op Amp. from -40°C to 125°C
Input frequency	Fain	-	-	8	MHz	Dependant upon CAM
Power supply rejection ratio	PSRR	N/A	N/A	N/A	dB	See CAM Op Amp
Large signal harmonic distortion	Dist	-	85	-	dB	See CAM Op Amp
Input resistance	Rin	-	-	-	Mohm	• Input to CAM directly (Input cell bypass mode) • This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture
Input capacitance	Cin	-	-	-	pF	• Input to CAM directly (Input cell bypass mode) • This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture

Analog Outputs

(See "Output Cell" section in the AN121E04/AN221E04 user manual for more details)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High precision output range [c]	Vouta	0.5	-	3.5	V	VMR +/- 1.5v
Reduced precision output range [d]	Vouta	0.1	-	3.9	V	VMR +/- 1.9v
High precision differential output [c]	Vdiffouta	-	-	+/-3.0	V	Common mode voltage = 2 V
Reduced precision differential output [d]	Vdiffouta	-	-	+/-3.8	V	Common mode voltage = 2 V
Common mode voltage	Vcm	1.9	2.0	2.1	V	
Noise figure	Noise	-	TBD	-	nV/sqrtHz	See typical graphical data provided later in this document
Signal-to noise ratio and distortion	SINAD	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660Hz • See typical graphical data provided later in this document
Spurious free dynamic range	SFDR	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660H • See typical graphical data provided later in this document

[c] High precision operating range provides optimal linearity and dynamic range
[d] Reduced precision operating range provides maximum dynamic range and reduced linearity

Output Voltage mode and filter ON, corner frequency 470kHz

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above			V	
Equivalent input offset	Vos	-	5	15	mV	
Offset voltage temperature coefficient	Voffsettc		0.05 [I]	1.0 [II]	mV/°C	from -40°C to 125°C I. measured at filter corner = 470kHz II. maximum at Filter corner = 76kHz
Output frequency	Fain	-	-	-	MHz	• Output filter frequency will define the maximum frequency • Input filter is recommended to be >30x higher then the max input frequency, for good distortion performance
Power supply rejection ratio	PSRR	60	-	-	dB	d.c. a.c. graphs
Large signal harmonic distortion	Dist	-	82	-	dB	4v p-p differential input at 660Hz Filter corner frequency 470kHz
Input low pass filter (anti-alais) Corner frequency settings	Ffiltcorner	76	-	470	kHz	
Output load [c e]	Rload	0.1	-	-	Mohm	
Output load [c e]	Cload	-	-	50	pF	
Output load [d e]	Rload	1	10	-	Kohm	• Additional loading causes internal voltage drops across output stage and series resistances • The output stage has a small signal output impedance of approx 10ohm
Output load [d e]	Cload	-	-	100	pF	

[c] High precision operating range provides optimal linearity and dynamic range
[d] Reduced precision operating range provides maximum dynamic range and reduced linearity
[e] The maximum load for an analog output is 50 pF || 100 Kohms. This load maybe with respect to analog ground VMR or AVSS

Output Voltage Mode and Filter Off (Bypass Mode)

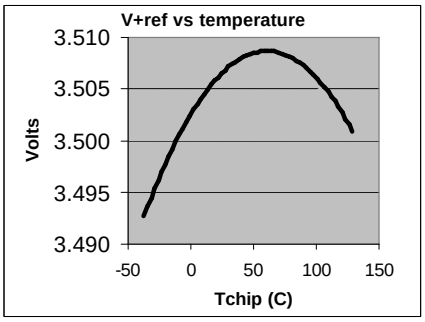
Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vina Vdiffina	See analog input above			V	
Equivalent input offset	Vos	N/A	N/A	N/A	mV	See CAM Op Amp
Offset voltage temperature coefficient	Voffsettc	N/A	N/A	N/A	mV/°C	See CAM Op Amp
Output frequency [c]	Fain	-	-	4	MHz	
Output frequency [d]	Fain	-	-	8	MHz	
Power supply rejection ratio	PSRR	N/A	N/A	N/A	dB	See CAM Op Amp
Large signal harmonic distortion	Dist	-	85	-	dB	
Output load	Rload	N/A	N/A	N/A	Mohm	See CAM Op Amp
Output load	Cload	N/A	N/A	N/A	pF	See CAM Op Amp

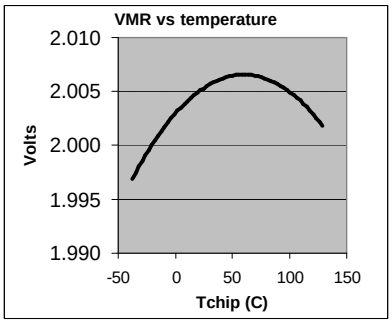
[c] High precision operating range provides optimal linearity and dynamic range

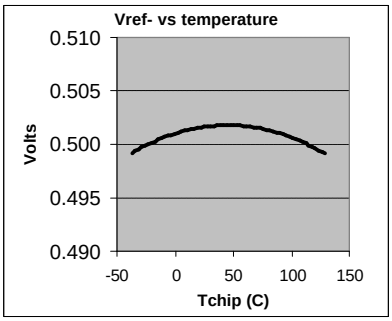
[f] The maximum load for an analog output is 100 pF || 100 Kohms. This load must be differential and with respect to analog ground(VMR)

VMR (Voltage Mid Rail) and VREF (Reference Voltage) Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VMR output voltage	Vvmr	1.925	2.01	2.075	V	At 25°C, Vdd=5.00 volts
VREF+ output voltage	Vref+	3.4	3.51	3.6	V	At 25°C, Vdd=5.00 volts
VREF- output voltage	Vref-	0.45	0.505	0.55	V	At 25°C, Vdd=5.00 volts
Output voltage deviation VREF+, VMR, VREF-	Vrefout	-	0.5	1	%	Over process and supply voltage corners
Voltage temperature coefficient VREF+, VMR, VREF-	Vreftc	-	-	-	-	See typical graphical data below -40°C to 125°C [f]
Power supply rejection ratio, VMR	PSSR	60	-	-	dB	
Power supply rejection ratio Vref+ and Vref-	PSSR	75	-	-	dB	
Start up time	Tstart	-	-	1	ms	Assuming recommended capacitors



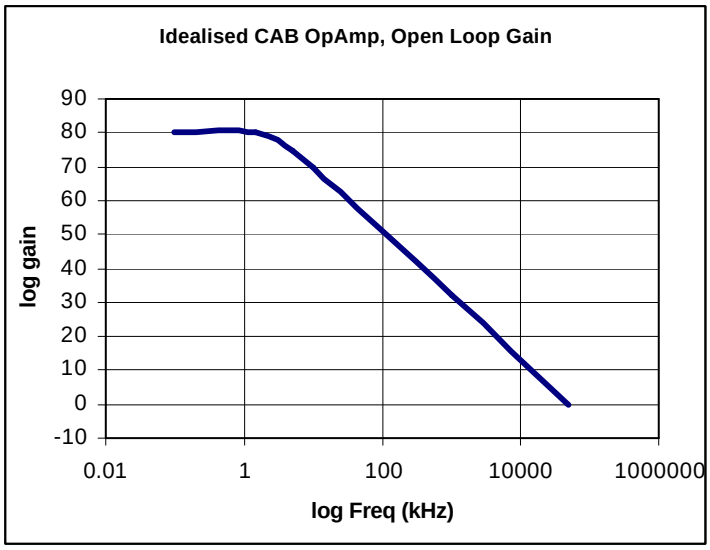




CAB (Configurable Analog Block) Differential Operational Amplifier

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High precision input/output range [c]	Vinouta	0.5	-	3.5	V	VMR +/- 1.5v
Reduced precision input/output range [d]	Vinouta	0.1	-	3.9	V	VMR +/-1.9v
High precision differential input/output [c]	Vdiffinouta	-	-	+/-3.0	V	Common mode voltage = 2 V
Reduced precision differential input/output [d]	Vdiffinouta	-	-	+/-3.8	V	Common mode voltage = 2 V
Common mode input voltage range [d]	Vcm	0	2.0	4	V	
Common mode output voltage range	Vcm	1.9	2.0	2.1	V	
Equivalent input voltage offset.	Voffset	0.1	5	15	mV	Some CAM's (Configurable Analog Modules) can inherently compensate
Offset voltage temperature coefficient	Voffsettc	-	1	10	µV/°C	from -40°C to 125°C some CAM's (Configurable Analog Modules) can inherently compensate
Power supply rejection ratio	PSSR	-	80	-	dB	Variation between CAM's is expected because of variations in architecture
Differential slew rate, internal	Slew	-	50	-	V/µsec	Applicable when the OpAmp load is internal to the FPAA
Differential slew rate, external	Slew	-	10	-	V/µsec	Applicable when the OpAmp driving signal out of the FPAA package
Unity gain bandwidth, full power mode.	UGB	-	50	-	MHz	Applicable when sourcing and loading the OpAmp with a load internal to the FPAA
Input impedance, internal	Rin	10	-	-	Mohm	
Output impedance, internal	Rout	-	-	-	Ohms	The OpAmp output is designed to drive all internal nodes, these are dominantly capacitive loads
Output impedance, external	Rout	-	-	-	Ohms	Output to an FPAA output pin (ouput cell bypass mode). This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture
Output load, external [ce]	Rload	0.1	-	-	Mohm	
Output load, external [ce]	Cload	-	-	50	pF	
Output load, external [def]	Rload	1	10	-	Kohm	• Additional loading causes internal voltage drops across output stage and series resistances • The output stage has a small signal output impedance of approx 10ohm
Output load, external [def]	Cload	-	-	50	pF	
Noise figure	Noise	-	TBD	-	nV/sqrtHz	See typical graphical data provided later in this document
Signal-to noise ratio and distortion	SINAD	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660Hz • See typical graphical data provided at the end of the document
Spurious free dynamic range	SFDR	-	TBD	-	dB	• VMR 2.0V, input signal =0.7v p-p differential, 660Hz • See typical graphical data provided at the end of the document

[c] High precision operating range provides optimal linearity and dynamic range
[d] Reduced precision operating range provides maximum dynamic range and reduced linearity
[e] The maximum load for an analog output is 50 pF || 100 Kohms. This load may be with respect to analog ground VMR or AVSS
[f] Using the FPAA with CAB Op Amp's driving directly off-chip, requires care, full characterization of the performance of each application circuit by the circuit designer is necessary



The idealized open loop gain plot is provided for information only. This information is associated with the FPAA in full power mode of operation. The FPAA operation amplifier open loop gain cannot be observed nor used when associated with external connections to the device. Internal reprogrammable routing impedances and switched capacitor circuit architecture using this operational amplifier limit the effective usable bandwidth of a circuit realized in the FPAA to less than 2MHz.

CAB (Configurable Analog Block) Differential Comparator

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range, internal	Vina	0.1	-	3.9	V	
Input range, external	Vina	0.0	-	Vdd	V	
Differential input, internal	Vdiffina	-	-	+/-3.8	V	Common mode voltage = 2 V
Differential input, external	Vdiffina	+/- 0.0	-	+/- Vdd	V	
Common mode input voltage range, external [c]	Vcm	0	2.0	4	V	
Common mode input voltage, external. [d]	Vcm	0	-	5	V	The comparator will function correctly
Differential output	Voutdiff	-	-	+/-5	V	
Single pin output (Ox1P)	Vout	0	-	5	V	
Input voltage offset	Voffsetcomp	-	2	10	mV	Zero hysterisis
Offset voltage temperature coefficient	Voffsettc	-	1	10	µV/°C	from -40°C to 125°C, Zero hysterisis
Setup time, internal	Tsetint	-	-	125	nsec	
Setup time, external	Tsetext	-	-	500	nsec	
Delay time	Tdelay	1/2 Td+25	-	1 1/2 Td+25	nsec	Td = 1/Fc Fc = master clock frequency
Output load	Rload	N/A	N/A	N/A	Mohm	
Output load	Cload	N/A	N/A	N/A	pF	
Differential variable reference voltage settings	CompVref	0	-	+/-4.0	V	
Differential hysteresis	Hysta1	-	Voffsetcomp	-	mV	Hysteresis setting = zero
Differential hysteresis	Hysta2	-	20	-	mV	Hysteresis setting = 10mV
Differential hysteresis	Hysta3	-	40	-	mV	Hysteresis setting = 20mV
Differential hysteresis	Hysta4	-	80	-	mV	Hysteresis setting = 40mV
Hysteresis setting accuracy	Hystb	-	25	-	%	
Hysteresis temperature coefficient	Hysttc1	-	5	-	µV/°C	Hysteresis setting = zero
Hysteresis temperature coefficient	Hysttc2	-	50	-	µV/°C	Hysteresis setting = 10mV
Hysteresis temperature coefficient	Hysttc3	-	100	-	µV/°C	Hysteresis setting = 20mV
Hysteresis temperature coefficient	Hysttc4	-	200	-	µV/°C	Hysteresis setting = 40mV

[c] High precision operating range provides optimal linearity and dynamic range
[d] Reduced precision operating range provides maximum dynamic range and reduced linearity

ESD Characteristics

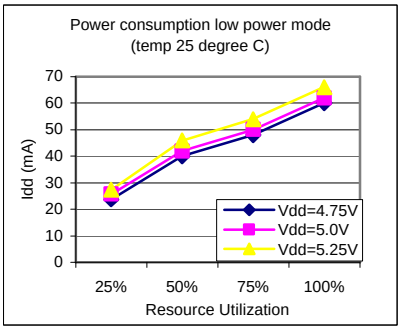
Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital inputs	4000V	250V	4kV
Digital outputs	4000V	250V	4kV
Digital bidirectional	4000V	250V	4kV
Digital open drain	4000V	250V	4kV
Analog Inputs	2000V	200V	4kV
Analog outputs	1500V	100V	4kV
Reference voltages	1500V	100V	4kV

The AN221E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN221E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Power Consumption – Low Power Mode

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Minimum power [1a]	Idd	-	0.2	-	mA	VDD=5.00 volts, Tj=25°C
Nominal 25% power[1b]	Idd	-	25	30	mA	VDD=5.00 volts, Tj=25°C
Nominal 50% power [1c]	Idd	-	42	47	mA	VDD=5.00 volts, Tj=25°C
Nominal 75% power[1d]	Idd	-	50	55	mA	VDD=5.00 volts, Tj=25°C
Maximum power[1e]	Idd	-	60 63 66	- 68 -	mA	VDD=4.75 volts, Tj=85°C VDD=5.00 volts, Tj=25°C VDD=5.25 volts, Tj= -40°C
Temperature coefficient	-	-	-2	-10	µA/°C	

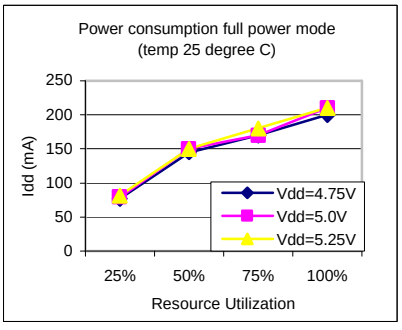
1a External clock, all analog function disabled, memory active
1b FPAA active elements – Two core op-amps (low power mode), one comparator, one input (bypass mode), one output filter and differential to single-ended converter (low power mode)
1c FPAA active elements – Four core op-amps (low power mode), two comparators (one using SAR), two inputs (bypass mode), two output filters and two differential to single-ended converters (low power mode)
1d FPAA active elements – Six core op-amps (low power mode), three comparators (two using SAR), three inputs (bypass mode, two output filters and two differential to single-ended converters (low power mode)
1e FPAA active elements – Eight core op-amps (low power mode), four comparators (two using SAR), four inputs (bypass mode), two output filters and two differential to single-ended converters (low power mode)



Power Consumption – Full Power Mode

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Full power mode minimum power [2a]	Idd	-	1.5	-	mA	VDD=5.00 volts, Tj=25°C
Full power mode nominal 25% power [2b]	Idd	-	80	90	mA	VDD=5.00 volts, Tj=25°C
Full power mode nominal 50% power [2c]	Idd	-	150	160	mA	VDD=5.00 volts, Tj=25°C
Full power mode nominal 75% power [2d]	Idd	-	170	190	mA	VDD=5.00 volts, Tj=25°C
Full power mode maximum power [2e]	Idd	-	200 210 220	- 230 -	mA	VDD=4.75 volts, Tj=85°C VDD=5.00 volts, Tj=25°C VDD=5.25 volts, Tj= -40°C

2a AN221E04 Crystal Oscillator, all analog functions disabled, memory active
2b FPAA active elements – Two core op-amps, one comparator, one input filter and chopper amplifier, one output filter and differential tosingle-ended converter
2c FPAA active elements – Four core op-amps, two comparators (one using SAR), two Input filters and two chopper amplifiers, two output filters and two differential to single-ended converters
2d FPAA active elements – Six core op-amps, three comparators (two using SAR), three input filters and three chopper amplifiers, two output filters and two differential to single-ended converters
2e FPAA active elements – Eight core op-amps, four comparators (two using SAR), four input filters and two chopper amplifiers, two output filters and two differential to single-ended converters



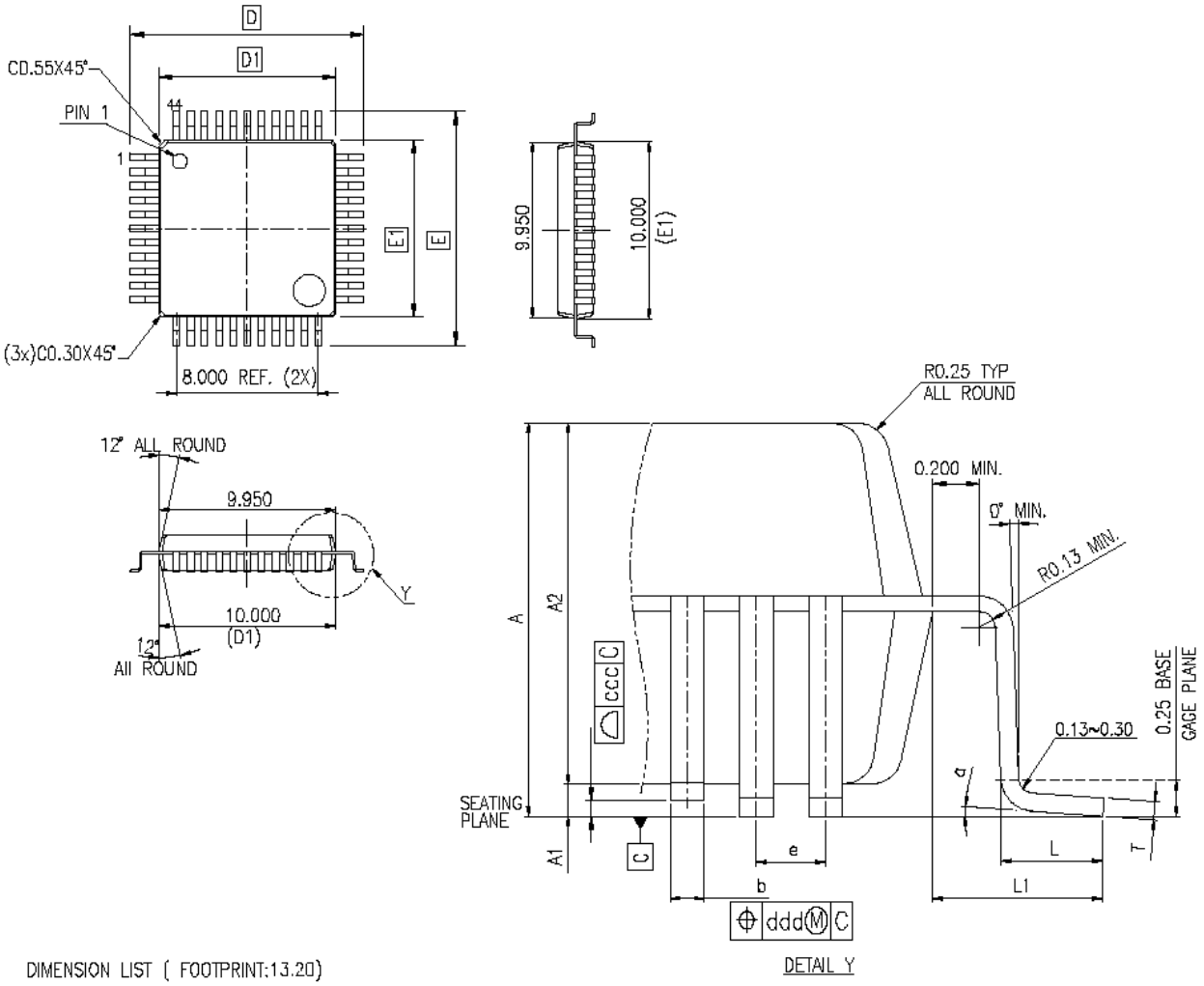
PINOUT

Pin Number	Pin Name	Pin Type	Comments
1	IO4PA	Analog IN+	
2	IO4NA	Analog IN-	
3	O1P	Analog OUT+	
4	O1N	Analog OUT-	
5	AVSS	Analog VSS	
6	AVDD	Analog VDD	
7	O2P	Analog OUT	
8	O2N	Analog OUT	
9	IO1P	Analog IN+	
10	IO1N	Analog IN-	
11	IO2P	Analog IN+	
12	IO2N	Analog IN-	
13	SHIELD	Analog VDD	Low noise VDD bias for capacitor array n-wells
14	AVDD2	Analog VDD	Analog Power
15	VREFMC	Vref	Attach filter capacitor for VREF-
16	VREFPC	Vref	Attach filter capacitor for VREF+
17	VMRC	Vref	Attach filter capacitor for VMR (Voltage Main Reference)
18	BVDD	Analog VDD	Analog power for Bandgap Vref generators
19	BVSS	Analog VSS	Analog ground for Bandgap Vref generators
20	CFGFLGb	Digital IN	In multi-device systems... 0, Ignore incoming data (unless currently addressed) 1, Pay attention to incoming data (watching for address)
		Digital OUT	0, Device is being configured Z, Device is not being configured (if internal pullup is selected)
21	CS2b	Digital IN	0, Chip is selected 1, Chip is not selected
22	CS1b	Digital IN (during config)	0, Allow configuration to proceed 1, Hold off configuration
		Digital IN (after config)_	Passes read-back data through to LCC_B pin
23	DCLK	Digital IN	
24	SVSS	Digital VSS	Digital ground - substrate tie
25	MODE	Digital IN	0, Synchronous serial interface 1, SPI EPROM interface
26	ACLK / SPIP	Digital IN	MODE = 0, Analog Clock < 40 MHz
		Digital OUT	MODE = 1, SPI EPROM or Serial EPROM Clock
27	OUTCLK / SPIMEM	Digital OUT	During power-up, sources SPI EPROM initialization command string
		Digital OUT	After power-up, sources any of the four internal analog clocks
28	DVDD	Digital VDD	
29	DVSS	Digital VSS	
30	DIN	Digital IN	Serial configuration data input
31	LCCb	Digital OUT	1, Local configuration is needed. Once configuration is completed, it is a registered version of CS1b or if the device is addressed for read, it serves as serial data out port
32	ERRb	Digital IN (monitored OUT)	0, Initiate reset 1, No action
		Digital OUT	0, Error condition Z, No error condition (external pullup required)
33	ACTIVATE	Digital IN	0, Hold off completion of configuration Rising edge, allow completion of configuration O.D. Output 0, Device has not yet completed primary configuration Z, Device has completed primary configuration (if internal pullup is selected)
34	DOUTCLK / TEST	Digital OUT	A buffered version of DCLK.
		Digital IN	(Factory reserved test input. Float if unused)
35	PORb	Digital IN	0, Chip Held in reset state Rising edge, re-initiates power on reset sequence
36	EXECUTE	Digital IN	0, No action 1, Transfer shadow RAM into configuration RAM
37	IO3P	Analog IN+	
38	IO3N	Analog IN-	
39	IO4PD	Analog IN+	Analog multiplexer input signals. The multiplexer can accept 4 differential inputs or 8 single ended inputs
40	IO4ND	Analog IN-	
41	IO4PC	Analog IN+	
42	IO4NC	Analog IN-	
43	IO4PB	Analog IN+	
44	IO4NB	Analog IN-	

This information is preliminary information — subject to change

MECHANICAL AND HANDLING

The AN221E04 comes in the industry standard 44 lead QFP package.
Dry pack handling is recommended. The package is qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.



DIMENSION LIST (FOOTPRINT:13.20)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 2.450	OVERALL HEIGTH
2	A1	MAX. 0.500	STANDOFF
3	A2	2.000±0.200	PKG THICKNESS
4	D	13.200±0.250	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	13.200±0.250	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WIDTH
8	L	0.880±0.150	FOOT LENGTH
9	L1	1.600 REF.	LEAD LENGTH
10	T	0.130~0.230	FRAME THICKNESS
11	α	0~7°	LEAD FLAT ANGLE
12	b	0.300~0.450	LEAD WIDTH
13	e	0.800 BASE	LEAD PITCH
14	ccc	0.100	FOOT PLANARITY
15	ddd	0.100	FOOT POSITION

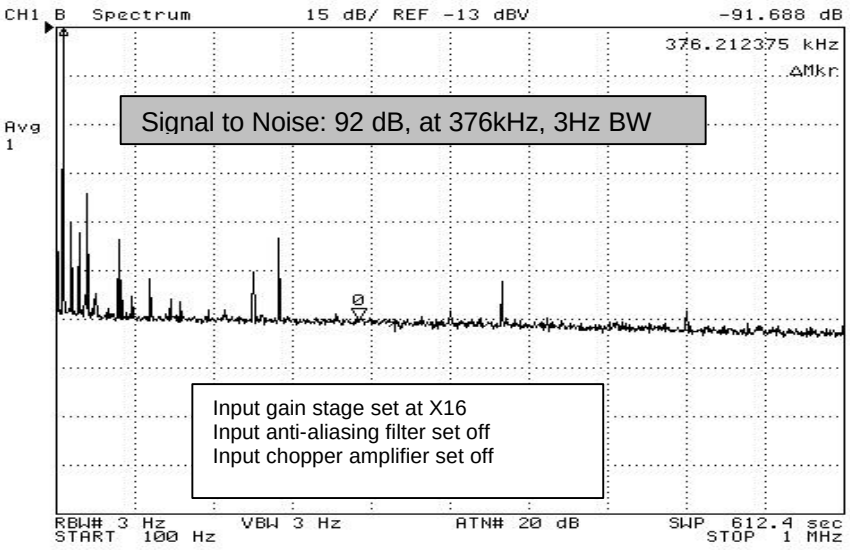
NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXPECT EJECTION AND PIN 1 MARKING.		Ra1.5~2.5um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-022		

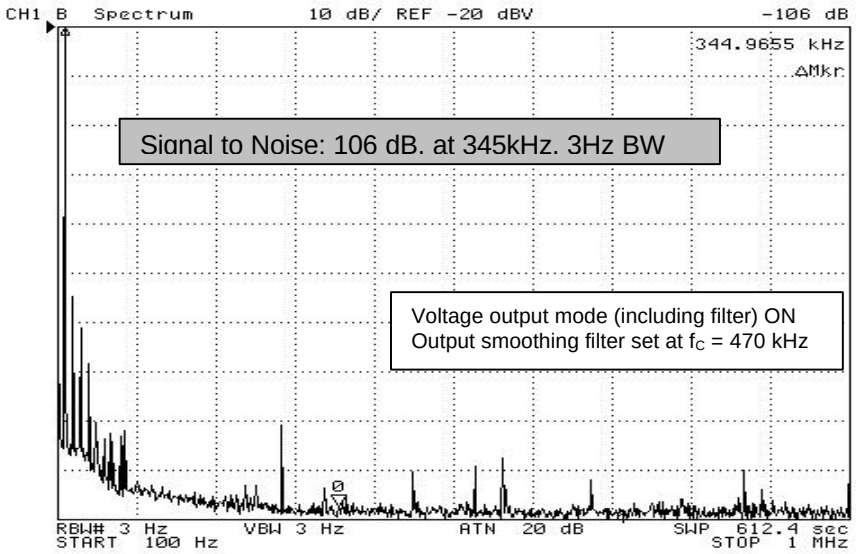
Noise and Distortion Observations

The following plots give an indication of the noise characteristics of Anadigm's AN221E04 FPAA device.
These were done using a simple set-up and in many cases reflect the noise limit of the setup. Actual device noise margins are expected to be better.

Signal and noise for the input cell (input signal - 50mVp-p differential to the FPAA at 10 kHz)



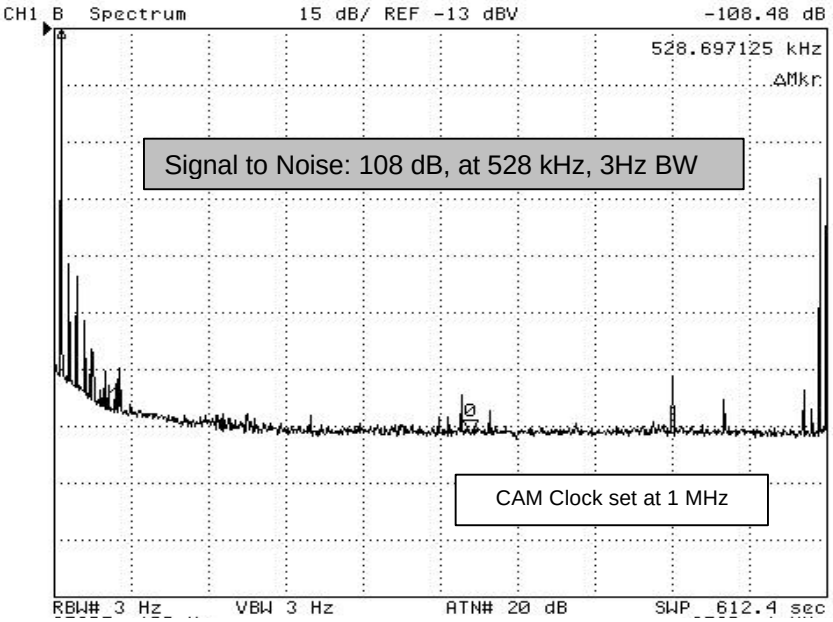
Signal and noise for the output cell (with a differential input 4V p-p, 660Hz)

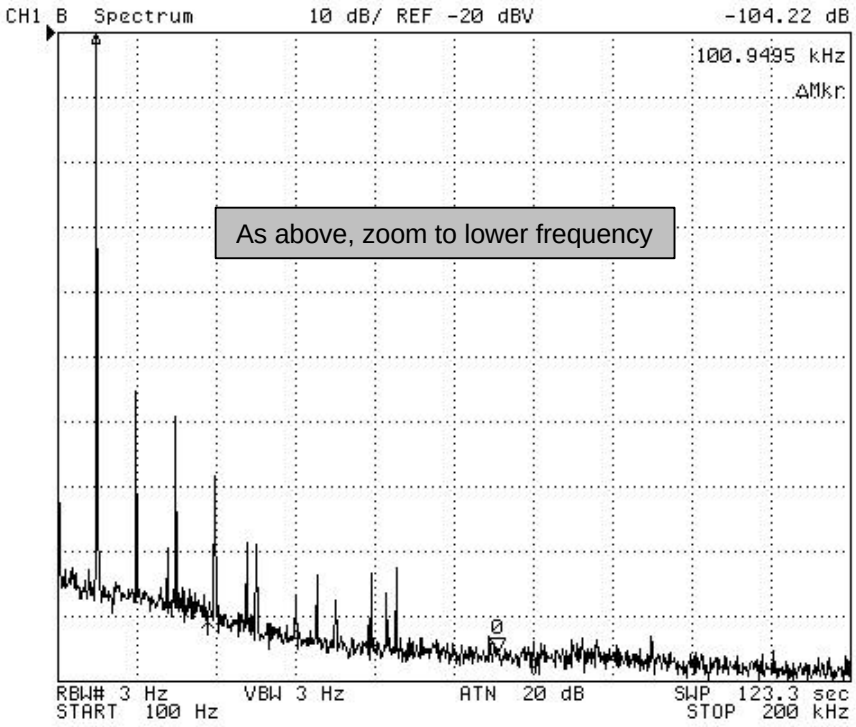


Measured THD for input and output cells (with a differential input 4V p-p, 660Hz)

Settings	Distortion in dB
Input cell with anti-aliasing filter set at f_C = 470 kHz	81.6
Output cell with differential to single ended converter and output smoothing filter set at f_C = 470 kHz	82

Signal and noise for a representative CAM – Gaininv CAM (input signal of 700mV p-p differential at 10 kHz)





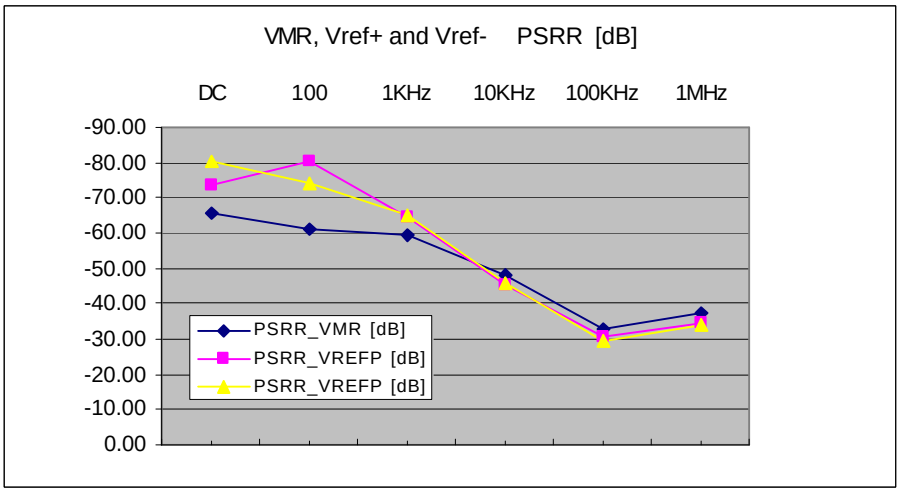
THD for a representative CAM – Gaininv CAM (with a differential input 4V p-p, 660Hz)

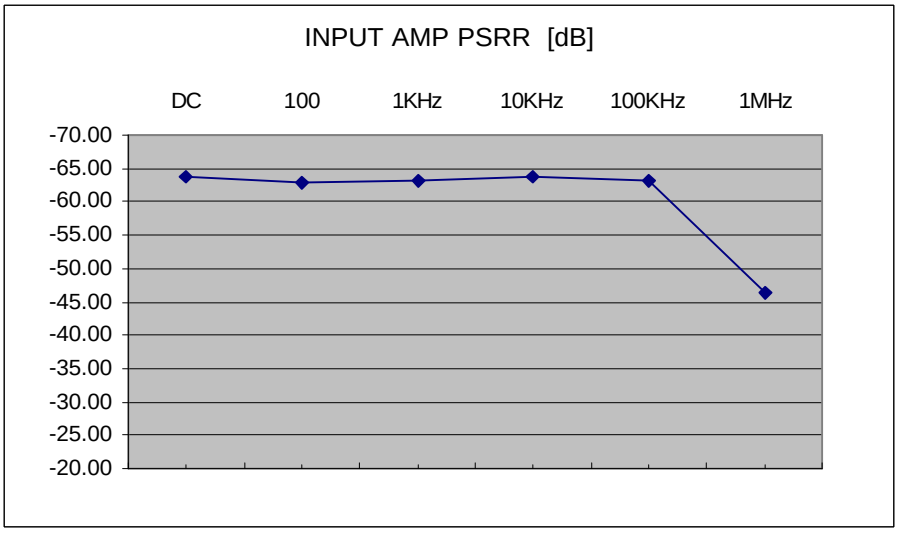
CAM Clock Frequency	Distortion (dB)
250 kHz	80.00
1 MHz	72.83
2 MHz	69.22
4 MHz	73.48

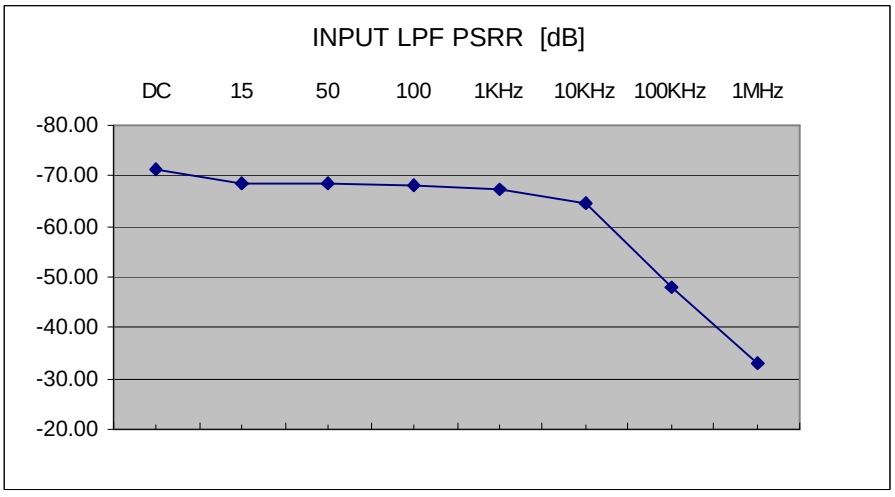
Power Supply Rejection Ratio (PSRR) Measurements

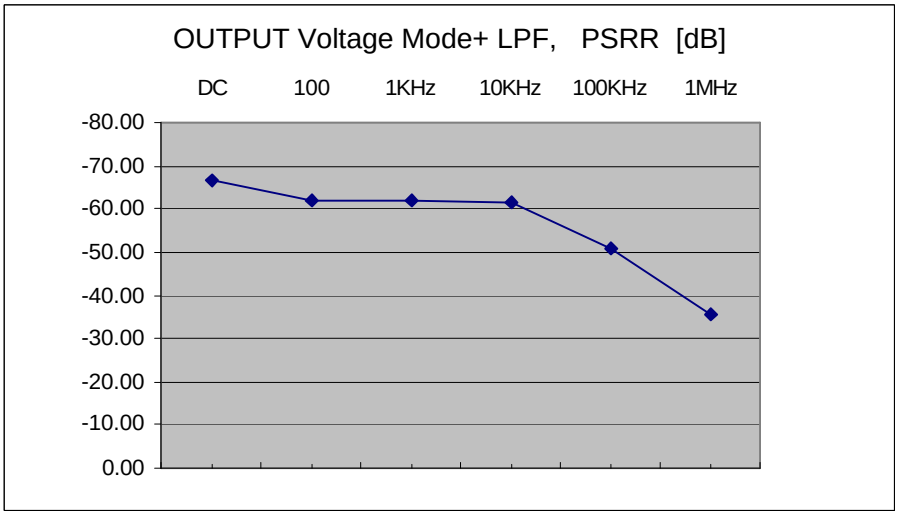
The following plots give an indication of the PSRR for some representative CAMs.

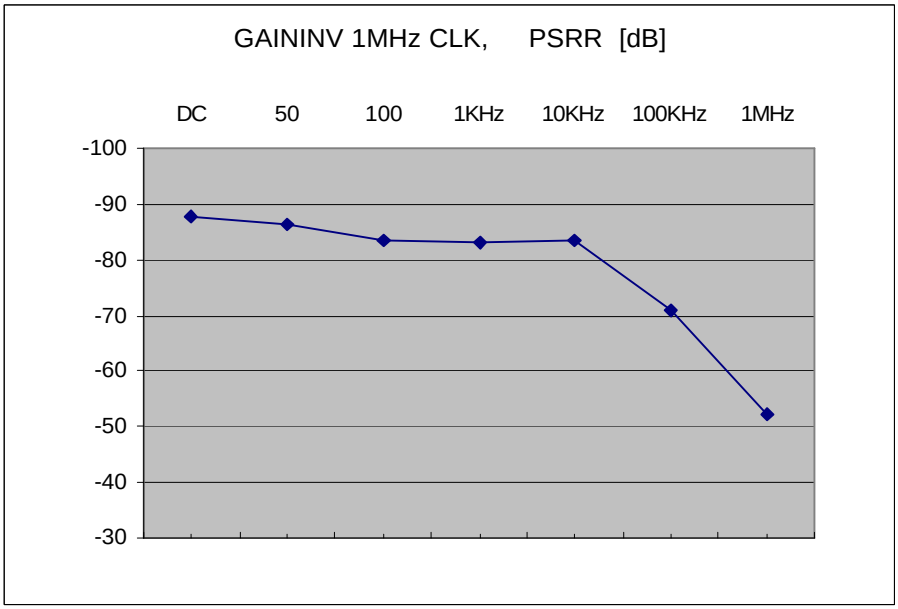
AVDD to Power Supply (PS): 5v +/- 0.25v sinusoidal waveform (100 kHz to 1 MHz)

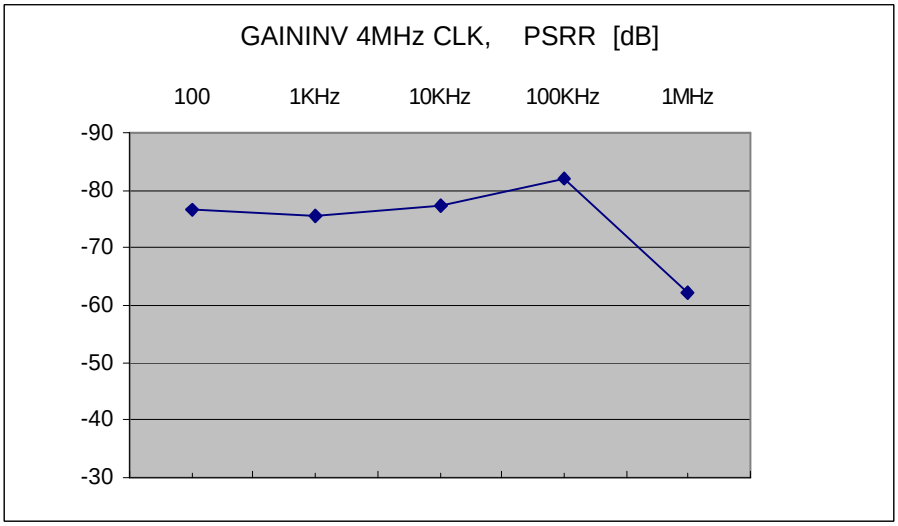







OUTPUT Voltage Mode+ LPF, PSRR [dB]
DC
100
1KHz
10KHz
100KHz
1MHz
-80.00
-70.00
-60.00
-50.00
-40.00
-30.00
-20.00
-10.00
0.00


GAININV 1MHz CLK, PSRR [dB]
DC
50
100
1KHz
10KHz
100KHz
1MHz
-100
-90
-80
-70
-60
-50
-40
-30


GAININV 4MHz CLK, PSRR [dB]
100
1KHz
10KHz
100KHz
1MHz
-90
-80
-70
-60
-50
-40
-30